Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A digital to analogue converter comprising:

a plurality of digital inputs ~~(D0-D5)~~ corresponding in number to the number of bits of a digital input word, the inputs being used to select one of first and second binary voltage levels ~~(VH,VL)~~ as binary inputs to the converter;

a respective capacitor circuit ~~(C, 2C, ... , 32C)~~ associated with each input;

first and second clock inputs ~~(CK1, CK2)~~;

an output load ~~(C_{LOAD})~~; and

a plurality of switches controlled by the clock inputs for controlling the coupling of the capacitor circuits either to one of the binary inputs or to the output load,

wherein ~~a plurality~~ each of the capacitor circuits [[are]] is controllable to output an effective voltage to the load, the effective voltage being selectable from at least three voltage levels comprising the first binary voltage level, the second binary voltage level or an average of the first and second binary voltage levels in dependence on the bits of the digital input word.

2. (Original) A converter as claimed in claim 1, wherein each capacitor circuit comprises an input circuit, having:

a first branch between a first input and the output and comprising first and second switches in series;

a second branch between a second input and the output and comprising third and fourth switches in series;

a capacitor connected between the junction between the first and second switches and the junction between the third and fourth switches.

3. (Currently Amended) A converter as claimed in claim 2, wherein the first and fourth switches are clocked by the first clock input [[(CK1)]] and the second and third switches are clocked by the second clock input [[(CK2)]].

4. (Currently Amended) A converter as claimed in claim 3, wherein the first and second clock inputs ~~(CK1, CK2)~~ are complementary signals.

5. (Previously Presented) A converter as claimed in claim 2, wherein each input circuit further comprises a first switching arrangement for supplying a first selected one of the binary voltage levels to the first input and a second switching arrangement for supplying a second selected one of the binary voltage levels to the second input.

6. (Original) A converter as claimed in claim 5, wherein the first and second switching arrangements of each of said plurality of the input circuits are controllable to provide the first binary voltage level to the first and second inputs, to provide the second binary voltage level to the first and second inputs, or to provide the first binary voltage level to one input and the second binary level to the other input.

7. (Currently Amended) A converter as claimed in claim 1, wherein the plurality of the capacitor circuits comprises all <u>of the capacitor circuits in the digital-to-analog converter except for</u> [[but]] one of the capacitor circuits.

8. (Currently Amended) A converter as claimed in claim 7, wherein said one [[input]] <u>capacitor</u> circuit is controlled by the most significant bit [[(D5)]] of the digital input word.

9. (Currently Amended) A converter as claimed in claim 8, wherein said one capacitor circuit is controllable to output an effective voltage comprising only the first binary voltage level [[(VH)]] or the second binary voltage level [[(VL)]].

10. (Previously Presented) A converter as claimed in claim 1, wherein the capacitor circuits are connected in parallel between the plurality of inputs and the capacitive output load.

11. (Original) A converter as claimed in claim 1, wherein each of the capacitor circuits comprises an input switch and an output switch in series between one of the binary inputs and the output load, and further comprising a capacitor connected between the junction between the input switch and output switch and a common terminal.

12. (Currently Amended) A converter as claimed in claim 11, wherein each input switch is controlled by the first clock input [[(CK2)]] and each output switch is controlled by the second clock input [[(CK1)]].

13. (Original) A converter as claimed in claim 12, further comprising an additional input switch and an additional output switch in series between the binary input associated with the most significant bit and the output load, the common terminal being defined at the junction between the additional input switch and the additional output switch.

14. (Currently Amended) A converter as claimed in claim 13, wherein the additional input switch is controlled by the second clock input [[(CK1)]] and the additional output switch is controlled by the first clock input [[(CK2)]].

15. (Currently Amended) A converter as claimed in claim 1, wherein each of the capacitor circuits comprises an input switch and an output switch in series between a first power

line [[(20)]] and a second power line [[(22)]], wherein the first power line is selectively connected to the first binary voltage level [[(VH)]] and the second power line is selectively connected to the second binary voltage level [[(VL)]], and further comprising a capacitor connected between the junction between the input switch and output switch and a common terminal.

16. (Currently Amended) A converter as claimed in claim 15, wherein the input switches are each controlled by a respective digital input ~~(DO - D5)~~ and the output switches are each controlled by the complement ~~(/D0 - /D5)~~ of the respective digital input.

17. (Currently Amended) A converter as claimed in claim 16, wherein the first and second power lines ~~(20,22)~~ are connected to the first and second binary voltage levels ~~(VH, VL)~~ under the control of one of the clock inputs [[(CK2)]], and the first and second power lines are connected to the output load under the control of the other one of the clock inputs [[(CK1)]].

18. (Currently Amended) A converter as claimed in claim 15, further comprising an additional input switch and an additional output switch in series between a third power line [[(24)]] and a fourth power line [[(26)]], the additional input switch and additional output switch are controlled by the most significant bit [[(D5)]] of the digital input, and the common terminal is defined at the junction between the additional input switch and the additional output switch.

19. (Currently Amended) A converter as claimed in claim 18, wherein the third and fourth power lines ~~(24,26)~~ are connected to the first and second binary voltage levels under the control of the other of the clock inputs [[(CK1)]], and the third and fourth power lines are connected to the output load under the control of the one of the clock inputs [[(CK2)]].

20. (Previously Presented) A converter as claimed in claim 1, wherein each capacitor circuit has an effective resistance determined by the capacitance.

21. (Currently Amended) A converter as claimed in claim 20, wherein the capacitor circuits have effective resistances ~~(R, 2R, ... , 32R)~~ such that they form a binary weighted circuit configuration.

22. (Currently Amended) A converter as claimed in claim 21 ,wherein the capacitor circuit with greatest effective resistance [[(32R)]] is controlled by the most significant bit [[(D5)]] of the digital input word, and the other capacitor circuits are each controlled by the most significant bit [[(D5)]] of the digital input word and one respective other bit [[(D0 - D4)]] of the digital input word.

23. (Currently Amended) A converter as claimed in claim 22, wherein:

the capacitor circuit with greatest effective resistance [[(32R)]] is controlled effectively to output either the first binary voltage level [[(VH)]] or the second binary voltage level [[(VL)]] in dependence on the most significant bit; and

each of the other capacitor circuits are controlled effectively to output:

either the second binary voltage level [[(VH)]] or the average of the first and second binary voltage levels when the most significant bit [[(D5)]] of the digital input word is high, in dependence on the respective other bit; or

either the first binary voltage level [[(VL)]] or the average of the first and second binary voltage levels when the most significant bit [[(D5)]] of the digital input word is tow, in dependence on the respective other bit.

24. (Previously Presented) A converter as claimed in claim 1, wherein the capacitor circuits are connected in parallel between the plurality of inputs and junctions of a resistor chain (R), a first end of the resistor chain being connected to the output load.

25. (Currently Amended) A converter as claimed in claim 24, wherein the capacitor circuits have the same effective resistances [[(2R)]].

26. (Currently Amended) A converter as claimed in claim 25, wherein the capacitor circuit at the second end of the resistor chain is controlled by the most significant bit [[(D5)]] of the digital input word, and the other capacitor circuits are each controlled by the most significant bit [[(D5)]] of the digital input word and one respective other bit ~~(D0 - D4)~~ of the digital input word.

27. (Currently Amended) A converter as claimed in claim 26, wherein:

the capacitor circuit at the second end of the resistor chain is controlled effectively to output either the first binary voltage level or the second binary voltage level in dependence on the most significant bit [[(D5)]]; and

each of the other capacitor circuits are controlled effectively to output:

either the second binary voltage level [[(VH)]] or the average of the first and second binary voltage levels when the most significant bit [[(D5)]] of the digital input word is high, in dependence on the respective other bit; or

either the first binary voltage level [[(VL)]] or the average of the first and second binary voltage levels when the most significant bit [[(D5)]] of the digital input word is low, in dependence on the respective other bit.

28. (Currently Amended) A converter as claimed in claim 25, wherein an average of the first and second binary voltage levels is coupled to the second end of the resistor chain through an effective resistance [[(2R)]] corresponding to the capacitor circuit effective resistance.

29. (Original) A converter as claimed in claim 28, wherein the average of the first and second binary voltage levels is coupled to the second end of the resistor chain by a further capacitor circuit.

30. (Currently Amended) A method of performing digital to analogue conversion, comprising:

using the bits of a digital input word to generate a plurality of control voltages corresponding in number to the number of bits, one control voltage comprising a first binary voltage level or a second binary voltage level, and each other control voltage <u>being selectable from at least three voltage levels</u> comprising a first binary voltage level, a second binary voltage level or an average of the first and second binary voltage levels; and

using the plurality of control voltages to drive an output load.

31. (Original) A method as c1aimed in claim 30, wherein generating a plurality of control voltage comprises operating a switched capacitor resistor circuit.

32. (Previously Presented) A method as claimed in claim 30, wherein generating a plurality of control voltage comprises operating a plurality of switched capacitor resistor circuits each having two control inputs, wherein one of the first and second binary voltage levels is applied to the first control input and one of the first and second binary voltage levels is applied to the second control input.

33. (Currently Amended) A display device comprising:

an array [[(34)]] of display pixels;

row driver circuitry [[(30)]] for providing signals to the rows of pixels; and

column address circuitry [[(32)]] providing pixel drive signals to the columns of pixels, wherein the column address circuitry [[(32)]] comprises a digital to analogue converter as claimed in claim 1.